AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-10 (Cancelled)

11. (Previously Presented) A non-volatile memory comprising an error correction circuit and a storage device,

wherein inputted data is written to said storage device corresponding to a first address, the written data is read from said storage device when a write error has occurred, said error correction circuit judges whether the read data can be corrected, a write operation ends if the read data can be corrected, said inputted data is written to said storage device corresponding to a second address which differs from said first address if the read data cannot be corrected.

12. (New) A nonvolatile memory comprising:

a plurality of nonvolatile memory cells; and

an error correcting circuit,

wherein address information and first data are received from outside,

wherein first nonvolatile memory cells of said plurality of nonvolatile memory cells are selected in accordance with said address information, and are programmed with said first data,

wherein second nonvolatile memory cells of said plurality of nonvolatile memory cells are selected, and second data stored therein are read out,

wherein said error correcting circuit judges whether said second data includes one or more correctable errors and corrects said second data when said second data includes one or more correctable errors, and

wherein said second nonvolatile memory cells are programmed with the corrected data.

13. (new) A nonvolatile memory according to claim 12, wherein after said first data is programmed and before said second nonvolatile memory cells are selected:

said first nonvolatile memory cells are selected and are read out,

said error correcting circuit judges whether data read out from said first nonvolatile memory cells includes errors which are not correctable by said error correcting circuit, and

programming of said first nonvolatile memory cells with said first data is completed if said read out data is judged to not include errors which are not correctable by said error correcting circuit.

14. (new) A nonvolatile memory according to claim 13,

wherein when said error correcting circuit judges that the data read out from said first memory cells includes errors which are not correctable by said error correcting circuit, third nonvolatile memory cells of said plurality of

nonvolatile memory cells different from said first nonvolatile memory cells are selected and are programmed with said first data.

15. (new) A nonvolatile memory according to claim 14, further including a buffer memory, and

wherein said first data is stored in said buffer memory until completion of programming with said first data.